What is claimed is:

1. A microprocessor comprising:

a processor core including an instruction executing unit configured to execute instructions for input and output controlling and processing for data and a cache memory configured to store the data;

a memory management unit coupled to the processor core, the memory management unit configured to manage memory system including the cache memory; and

a bus interface coupled to the processor core and the memory management unit, the bus interface configured to rearrange the bits of the data transferred from the processor core.

2. The microprocessor as claimed in claim 1, wherein the bus interface comprises:

a data input/output unit coupled to the processor core and memory management unit, the data input/output unit configured to receive and send the data;

a switching circuit coupled to the data input/output unit, the switching circuit configured to receive the data to change the order of bits of the data according to pre-routing information; and

a bus switch coupled to the switching circuit, the bus switch configured to receive the data changed order of bits to change the order of bits per predetermined number of the bits.

3. The microprocessor as claimed in claim 2, wherein the memory management unit comprises:

a pre-routing storing unit configured to store the pre-routing information that indicates the connection state of signals of the switching circuit; and

an address translation buffer configured to store information for translating virtual addresses generated inside the processor into physical addresses.

4. The microprocessor as claimed in claim 3, wherein the switching circuit changes connection state of signals according to the pre-routing information to change the order of bits.

5. The microprocessor as claimed in claim 4, wherein the pre-routing information is transferred from the memory management unit to the switching circuit when the data is to be outputted to a destination outside the processor.

6. The microprocessor as claimed in claim 2, wherein the switching circuit changes the order of bits of the data per a bit.

7. The microprocessor as claimed in claim 3, wherein the bus switch changes connection state of signals based on bus

switch control information to change the order of bits of the data.

8. The microprocessor as claimed in claim 7, wherein the bus switch control information is stored by the memory management unit.

9. The microprocessor as claimed in claim 2, wherein the bus switch changes the order of bits per a page managed by the memory management unit.

10. The microprocessor as claimed in claim 7, wherein the memory management unit stores the bus switch control information in each entry of the address translation cache memory.

11. The microprocessor as claimed in claim 7, wherein the bus switch control information is stored by an entry of the cache memory in the processor core.

12. The microprocessor as claimed in claim 9, wherein the bus switch receives the bus switch control information when an external address is accessed by the processor then the bus switch changes the order of bits of the data based on the bus switch control information.

13. The microprocessor as claimed in claim 20, wherein the memory management unit includes a bus switch control information storing unit storing the bus switch control information, the memory management unit transfers the bus switch control information corresponding to a physical address stored in the address transfer cache memory when an external address is accessed by the processor.

14. A video/sound processing system comprising:

a storage device configured to store content;

a bridge coupled to the storage device, the bridge configured to transfer the content stored by the storage device;

a microprocessor including:

a processor core including an instruction executing unit configured to execute instructions for input and output controlling and processing for the content and a cache memory configured to store the content;

a memory management unit coupled to the processor core, the memory management unit configured to manage memory system including the cache memory; and

a bus interface coupled to the processor core and the memory management unit, the bus interface configured to rearrange the bits of the content transferred from the processor core;

a memory coupled to the bridge, the memory configured to temporally hold the rearranged content from the micro

processor; and

a D/A converter coupled to the memory, the D/A converter configured to convert the transferred content to analog data.

15. The video/sound processing system as claimed in claim 14, wherein the bus interface comprises:

a data input/output unit coupled to the processor core and memory management unit, the data input/output unit configured to receive and send the content;

a switching circuit coupled to the data input/output unit, the switching circuit configured to receive the content to change the order of bits of the content according to pre-routing information; and

a bus switch coupled to the switching circuit, the bus switch configured to receive the content changed order of bits to change the order of bits per predetermined number of the bits.

16. The video/sound processing system as claimed in claim 15, wherein the memory management unit comprises:

a pre-routing storing unit configured to store the pre-routing information that indicates the connection state of signals of the switching circuit; and

an address translation buffer configured to store information for translating virtual addresses generated inside the

processor into physical addresses.

17. The video/sound processing system as claimed in claim 16, wherein the switching circuit changes connection state of signals according to the pre-routing information to change the order of bits of the content.

18. The video/sound processing system as claimed in claim 17, the pre-routing information is transferred from the memory management unit to the switching circuit when the content is to be outputted to a destination outside the processor.

19. The video/sound processing system as claimed in claim 15, wherein the switching circuit changes the order of bits of the content per a bit.

20. The video/sound processing system as claimed in claim 16, wherein the bus switch changes connection state of signals based on bus switch control information to change the order of bits of the content.